Proposed Instruction Encodings for the RISC-V Base P Extension

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Warning! This document is only a draft proposal and is not an official document of the RISC-V International Association. The Base P extension that is eventually ratified by RISC-V International is liable to differ from this proposal in many details.

This document proposes encodings for the instructions of the RISC-V Base P extension, both for RV32 and for RV64. For more about this proposal, see my other documents:

- *System for RISC-V P Extension Instruction Names*
- *Proposed Instructions for the RISC-V Base P Extension*

This version (020) differs from the previous one (019) with the addition of:

- SHL instructions (shift left or right, logical) that are unsigned versions of the SHA instructions (shift left or right, arithmetic); and
- for RV64 only, 'P'-suffix versions of PNCLIP instructions that are similar to RV32 PNCLIP instructions without shifting or rounding.

The complete set of instructions added for RV32 are:

PSSHL.HS	SSHL	PSSHL.DHS	PSSHL.DWS
PSSHLR.HS	SSHLR	PSSHLR.DHS	PSSHLR.DWS

And for RV64:

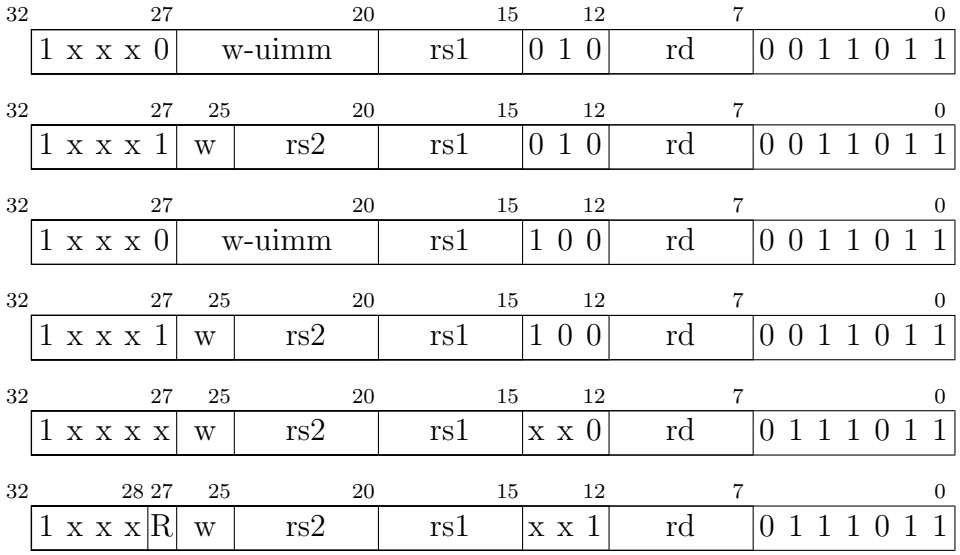
PSSHL.HS	PSSHL.WS	SHL	PNCLIPP.B	PNCLIPP.H	PNCLIPP.W
PSSHLR.HS	PSSHLR.WS	SHLR	PNCLIPUP.B	PNCLIPUP.H	PNCLIPUP.W

1 Instruction formats

A few non-SIMD instructions of the P extension (including ABS, CLS, PACK, REV, and REV16) are encoded alongside other ordinary RISC-V "scalar" instructions in the major opcodes known as OP (binary code 0110011), OP-IMM (0010011), and OP-IMM-32 (0011011).

All other Base P instructions are encoded either: (a) within major opcode OP-32 (binary code 0111011) with instruction bit 31 = 1; or (b) within OP-IMM-32 with bits 14:12 (func3) = binary 010, 100, or 110.

Apart from the subset of non-SIMD instructions already mentioned plus a few other special cases, the following instruction formats are used for all Base P instructions that have no register-pair operands, only single registers:

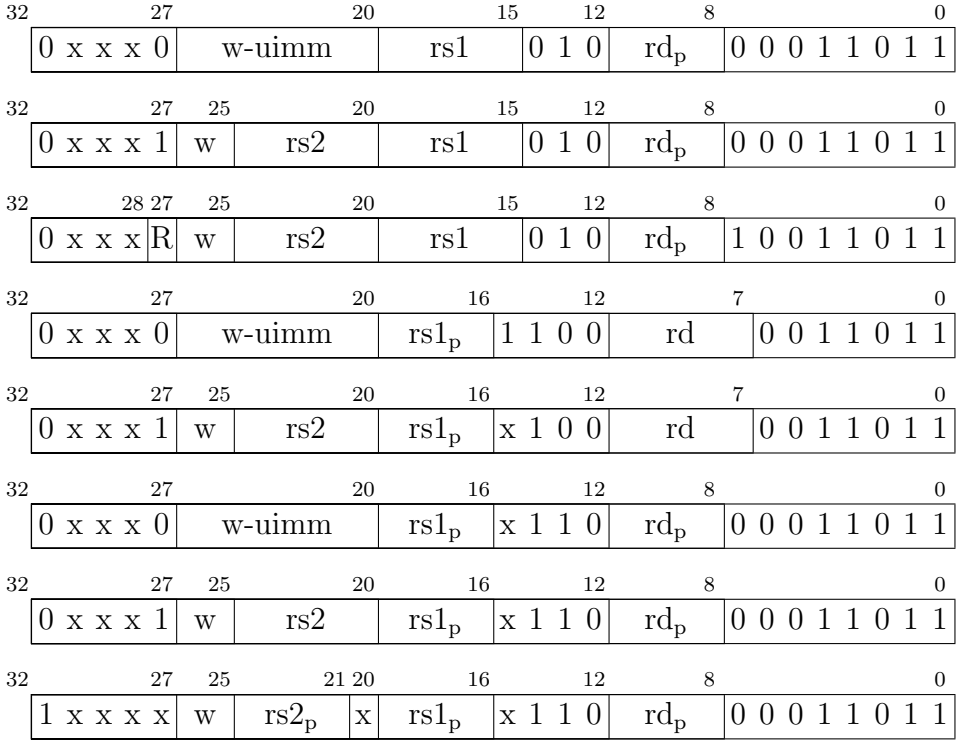


Note that the first four formats are in major opcode OP-IMM-32, and the last two are in OP-32. Of the OP-IMM-32 formats, those with func3 = binary 010 are mostly shifts left, while those with func3 = binary 100 are mostly shifts right.

The two-bit field w often selects the SIMD element width, whether bytes, halfwords, or words, although that is not its only function. The most common, though not universal, encoding for w has binary 00 = halfwords, 01 = words, 10 = bytes, and 11 = a doubleword. Field w-uimm encodes both an element width and an unsigned immediate operand whose size varies with the element width; for example, 3 bits for bytes, 4 bits for halfwords, 5 bits for words, and 6 bits for a doubleword.

For the last format, when bit R = 1, an instruction both reads and writes the destination operand. Usually this is done for an accumulate operation, although there are some other instances, such as SRX (Shift Right Extended) and MVM (Move Masked). Instructions encoded in the other formats listed above never read the destination.

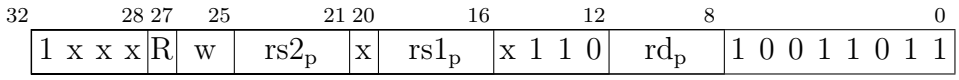
With RV32, the P extension has additional instruction formats for the cases when operands are even-odd register pairs:



All of these are in major opcode OP-IMM-32. The formats here with func3 = binary 010 primarily encode widening shifts left and other widening instructions, and those with func3 = binary 100 encode narrowing shifts right and reductions. The last three formats, with func3 = binary 110, encode all the double-wide instructions, which have at least the first source and destination as register pairs, and often the second source operand as well.

The third format listed above, with an R bit, encodes widening adds, subtracts, and multiplies that may optionally read the destination for an accumulate operation (WADDA, WSUBA, WMACC, etc.).

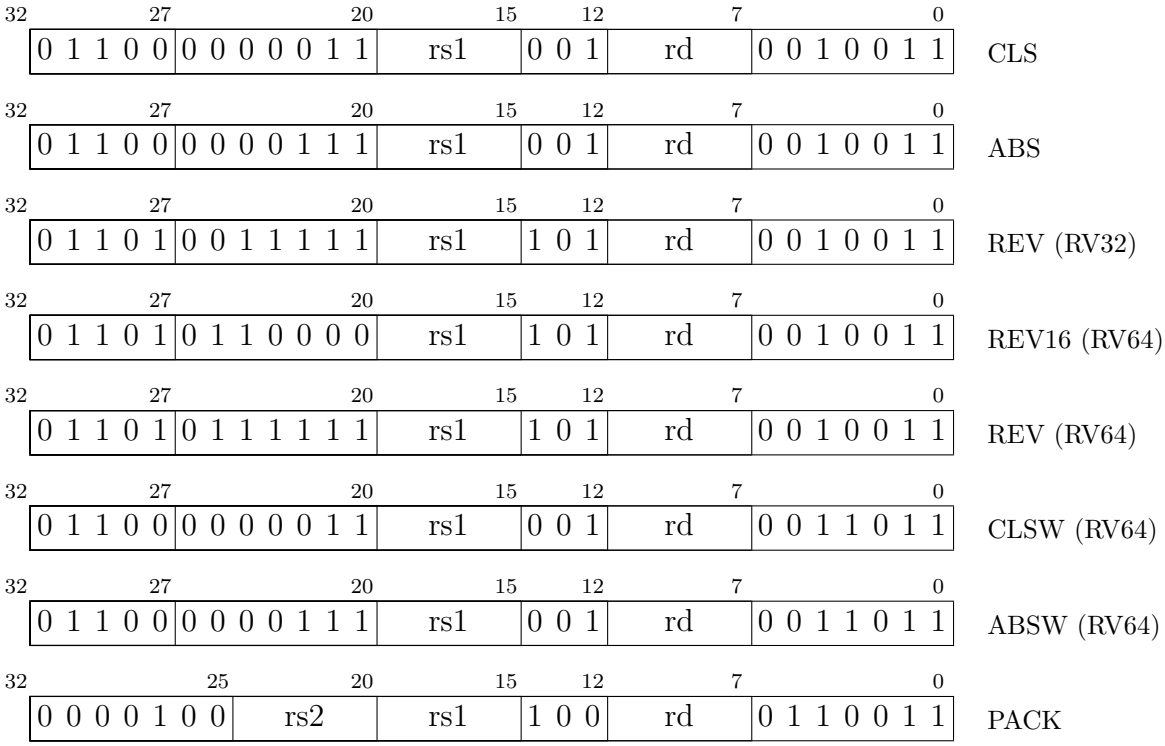
The following format is not used by Base P but is recommended for a Zp∗ extension that adds double-wide multiply instructions:

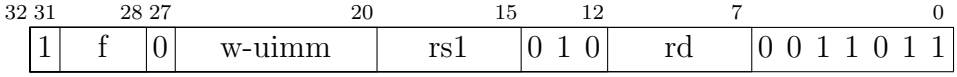


2 Encodings of instructions with no register-pair operands

In this section, all instruction tables show separately the allocations of instructions for RV32 and for RV64. Asterisks (*) mark where there are differences between the RV32 and RV64 halves of a table.

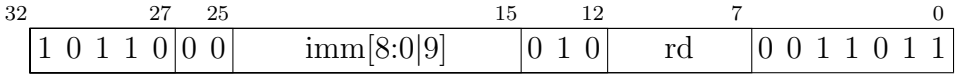
Where an instruction name is within braces { }, there is no such instruction proposed for the Base P extension, but the indicated encoding is recommended should the instruction be provided by another extension.



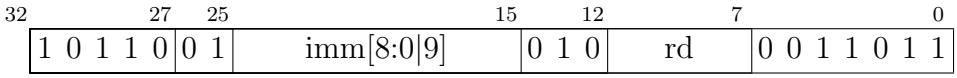


RV32 f	w-uimm 0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSLLI.B { PSSLLI.B }	PSLLI.H { PSSLLI.H }	* * { SSLLI }	
001					
010					
011	*PLI instructions*				
100					
101		{ PSSLAI.B }	PSSLAI.H	* SSLAI	
110	*unary instructions*				
111	*PLUI instructions*				

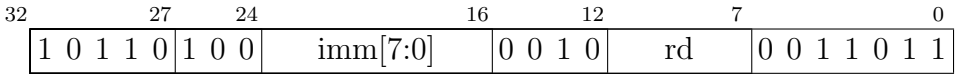
RV64 f	w-uimm 0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSLLI.B { PSSLLI.B }	PSLLI.H { PSSLLI.H }	* PSLLI.W * { PSSLLI.W }	
001					
010					
011	*PLI instructions*				
100					
101		{ PSSLAI.B }	PSSLAI.H	* PSSLAI.W	
110	*unary instructions*				
111	*PLUI instructions*				



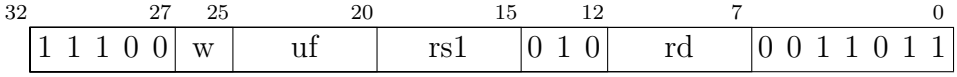
PLI.H



PLI.W (RV64)

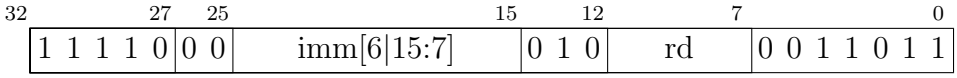


PLI.B

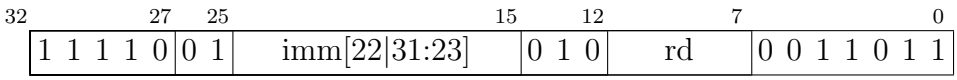


RV32	w			
uf	00	01	10	11
00000	{PCLZ.H}	*	{PCLZ.B}	
00001				
00010				
00011	{PCLS.H}	*	{PCLS.B}	
00100	PSEXT.H.B	*		
00101		*		
00110				
00111	PSABS.H	* {SABS}	PSABS.B	
01000				
01001				
01010				
01011				
...				
11111				

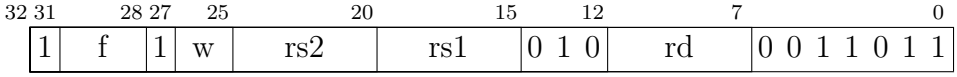
RV64	w			
uf	00	01	10	11
00000	{PCLZ.H}	* {PCLZ.W}	{PCLZ.B}	
00001				
00010				
00011	{PCLS.H}	* {PCLS.W}	{PCLS.B}	
00100	PSEXT.H.B	* PSEXT.W.B		
00101		* PSEXT.W.H		
00110				
00111	PSABS.H	* {PSABS.W}	PSABS.B	
01000				
01001				
01010				
01011				
...				
11111				



PLUI.H

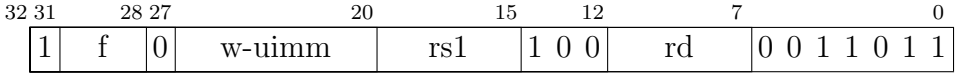


PLUI.W (RV64)



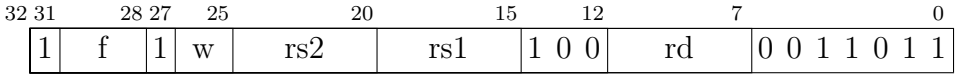
RV32	w			
f	00	01	10	11
000	PSLL.HS	*	PSLL.BS	
001	PADD.HS	*	PADD.BS	
010	PSSHL.HS	* SSHL	{ PSSHL.BS }	*
011	PSSHLR.HS	* SSHLR	{ PSSHLR.BS }	*
100				
101				
110	PSSHA.HS	* SSHA	{ PSSHA.BS }	*
111	PSSHAR.HS	* SSHAR	{ PSSHAR.BS }	*

RV64	w			
f	00	01	10	11
000	PSLL.HS	* PSLL.WS	PSLL.BS	
001	PADD.HS	* PADD.WS	PADD.BS	
010	PSSHL.HS	* PSSHL.WS	{ PSSHL.BS }	* SHL
011	PSSHLR.HS	* PSSHLR.WS	{ PSSHLR.BS }	* SHLR
100				
101				
110	PSSHA.HS	* PSSHA.WS	{ PSSHA.BS }	* SHA
111	PSSHAR.HS	* PSSHAR.WS	{ PSSHAR.BS }	* SHAR



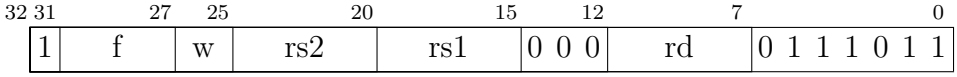
RV32 f	w-uimm 0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSRLI.B	PSRLI.H	*	
001		{ PSRLRI.B }	{ PSRLRI.H }	* { SRLRI }	*
010		{ PUSATI.B }	PUSATI.H	* USATI	*
011					
100		PSRAI.B	PSRAI.H	*	
101		{ PSRARI.B }	PSRARI.H	* SRARI	*
110		{ PSATI.B }	PSATI.H	* SATI	*
111					

RV64 f	w-uimm 0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSRLI.B	PSRLI.H	* PSRLI.W	
001		{ PSRLRI.B }	{ PSRLRI.H }	* { PSRLRI.W }	* { SRLRI }
010		{ PUSATI.B }	PUSATI.H	* PUSATI.W	* USATI
011					
100		PSRAI.B	PSRAI.H	* PSRAI.W	
101		{ PSRARI.B }	PSRARI.H	* PSRARI.W	* SRARI
110		{ PSATI.B }	PSATI.H	* PSATI.W	* SATI
111					



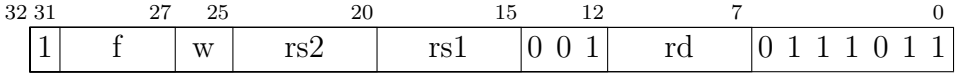
RV32 f	w 00	01	10	11
000	PSRL.HS	*	PSRL.BS	
001	PREDSUM.HS	*	PREDSUM.BS	
010				
011	PREDSUMU.HS	*	PREDSUMU.BS	
100	PSRA.HS	*	PSRA.BS	
101				
110				
111				

RV64 f	w 00	01	10	11
000	PSRL.HS	* PSRL.WS	PSRL.BS	
001	PREDSUM.HS	* PREDSUM.WS	PREDSUM.BS	
010				
011	PREDSUMU.HS	* PREDSUMU.WS	PREDSUMU.BS	
100	PSRA.HS	* PSRA.WS	PSRA.BS	
101				
110				
111				



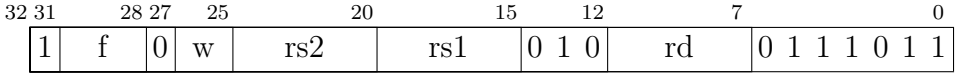
RV32	w			
f	00	01	10	11
0000	PADD.H	*	PADD.B	
0001				
0010	PSADD.H	* SADD	PSADD.B	
0011	PAADD.H	* AADD	PAADD.B	
0100				
0101				
0110	PSADDU.H	* SADDU	PSADDU.B	
0111	PAADDU.H	* AADDU	PAADDU.B	
1000	PSUB.H	*	PSUB.B	
1001	PABD.H	* { ABD }	PABD.B	
1010	PSSUB.H	* SSUB	PSSUB.B	
1011	PASUB.H	* ASUB	PASUB.B	
1100				
1101	PABDU.H	* { ABDU }	PABDU.B	
1110	PSSUBU.H	* SSUBU	PSSUBU.B	
1111	PASUBU.H	* ASUBU	PASUBU.B	

RV64	w			
f	00	01	10	11
0000	PADD.H	* PADD.W	PADD.B	
0001				
0010	PSADD.H	* PSADD.W	PSADD.B	
0011	PAADD.H	* PAADD.W	PAADD.B	
0100				
0101				
0110	PSADDU.H	* PSADDU.W	PSADDU.B	
0111	PAADDU.H	* PAADDU.W	PAADDU.B	
1000	PSUB.H	* PSUB.W	PSUB.B	
1001	PABD.H	* { PABD.W }	PABD.B	
1010	PSSUB.H	* PSSUB.W	PSSUB.B	
1011	PASUB.H	* PASUB.W	PASUB.B	
1100				
1101	PABDU.H	* { PABDU.W }	PABDU.B	
1110	PSSUBU.H	* PSSUBU.W	PSSUBU.B	
1111	PASUBU.H	* PASUBU.W	PASUBU.B	



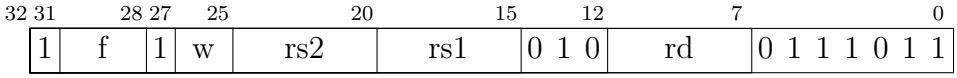
RV32 f	w 00	01	10	11
0000				
0001				SLX
0010	PMUL.H.B01	* MUL.H01		*
0011	{ PMACC.H.B01 }	* MACC.H01		*
0100				
0101	MVM	MVMN	MERGE	SRX
0110	PMULU.H.B01	* MULU.H01	PABDSUMU.B	*
0111	{ PMACCU.H.B01 }	* MACCU.H01	PABDSUMAU.B	*
1000				
1001				
1010				
1011				
1100				
1101				
1110				
1111				

RV64 f	w 00	01	10	11
0000				
0001				SLX
0010	PMUL.H.B01	* PMUL.W.H01		* MUL.W01
0011	{ PMACC.H.B01 }	* PMACC.W.H01		* MACC.W01
0100				
0101	MVM	MVMN	MERGE	SRX
0110	PMULU.H.B01	* PMULU.W.H01	PABDSUMU.B	* MULU.W01
0111	{ PMACCU.H.B01 }	* PMACCU.W.H01	PABDSUMAU.B	* MACCU.W01
1000				
1001				
1010				
1011				
1100				
1101				
1110				
1111				



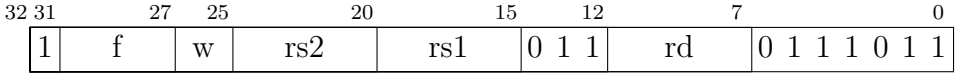
RV32	w			
f	00	01	10	11
000	*	*		*
001				
010	PSH1ADD.H	*		
011	PSSH1SADD.H	* SSH1SADD		
100	*	*		*
101				
110	* { UNZIP8P }	*	* { UNZIP8HP }	*
111	* { ZIP8P }	*	* { ZIP8HP }	*

RV64	w			
f	00	01	10	11
000	* PNCLIPUP.B	* PNCLIPUP.H		* PNCLIPUP.W
001				
010	PSH1ADD.H	* PSH1ADD.W		
011	PSSH1SADD.H	* PSSH1SADD.W		
100	* PNCLIPP.B	* PNCLIPP.H		* PNCLIPP.W
101				
110	* UNZIP8P	* UNZIP16P	* UNZIP8HP	* UNZIP16HP
111	* ZIP8P	* ZIP16P	* ZIP8HP	* ZIP16HP



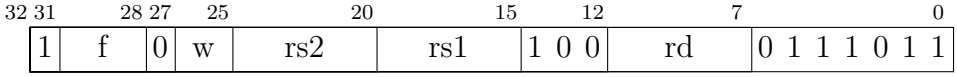
RV32	w			
f	00	01	10	11
000	{ PSLL.H }	*	{ PSLL.B }	
001				
010	{ PSSHL.H }	*	{ PSSHL.B }	
011	{ PSSHLR.H }	*	{ PSSHLR.B }	
100				
101				
110	{ PSSHA.H }	*	{ PSSHA.B }	
111	{ PSSHAR.H }	*	{ PSSHAR.B }	

RV64	w			
f	00	01	10	11
000	{ PSLL.H }	* { PSLL.W }	{ PSLL.B }	
001				
010	{ PSSHL.H }	* { PSSHL.W }	{ PSSHL.B }	
011	{ PSSHLR.H }	* { PSSHLR.W }	{ PSSHLR.B }	
100				
101				
110	{ PSSHA.H }	* { PSSHA.W }	{ PSSHA.B }	
111	{ PSSHAR.H }	* { PSSHAR.W }	{ PSSHAR.B }	



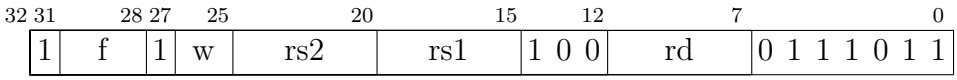
RV32	w			
f	00	01	10	11
0000	PMUL.H.B00	* MUL.H00		*
0001	{ PMACC.H.B00 }	* MACC.H00		*
0010	PMUL.H.B11	* MUL.H11		*
0011	{ PMACC.H.B11 }	* MACC.H11		*
0100	PMULU.H.B00	* MULU.H00		*
0101	{ PMACCU.H.B00 }	* MACCU.H00		*
0110	PMULU.H.B11	* MULU.H11		*
0111	{ PMACCU.H.B11 }	* MACCU.H11		*
1000				
1001				
1010				
1011				
1100	PMULSU.H.B00	* MULSU.H00		*
1101	{ PMACCSU.H.B00 }	* MACCSU.H00		*
1110	PMULSU.H.B11	* MULSU.H11		*
1111	{ PMACCSU.H.B11 }	* MACCSU.H11		*

RV64	w			
f	00	01	10	11
0000	PMUL.H.B00	* PMUL.W.H00		* MUL.W00
0001	{ PMACC.H.B00 }	* PMACC.W.H00		* MACC.W00
0010	PMUL.H.B11	* PMUL.W.H11		* MUL.W11
0011	{ PMACC.H.B11 }	* PMACC.W.H11		* MACC.W11
0100	PMULU.H.B00	* PMULU.W.H00		* MULU.W00
0101	{ PMACCU.H.B00 }	* PMACCU.W.H00		* MACCU.W00
0110	PMULU.H.B11	* PMULU.W.H11		* MULU.W11
0111	{ PMACCU.H.B11 }	* PMACCU.W.H11		* MACCU.W11
1000				
1001				
1010				
1011				
1100	PMULSU.H.B00	* PMULSU.W.H00		* MULSU.W00
1101	{ PMACCSU.H.B00 }	* PMACCSU.W.H00		* MACCSU.W00
1110	PMULSU.H.B11	* PMULSU.W.H11		* MULSU.W11
1111	{ PMACCSU.H.B11 }	* PMACCSU.W.H11		* MACCSU.W11



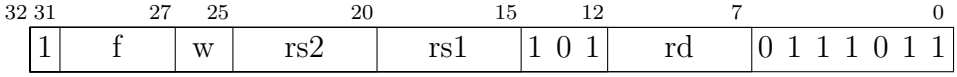
RV32	w			
f	00	01	10	11
000	PPAIRE.B	*		
001	PPAIREO.B	PPAIREO.H		*
010	PPAIROE.B	PPAIROE.H		*
011	PPAIRO.B	PPAIRO.H		*
100				
101				
110				
111				

RV64	w			
f	00	01	10	11
000	PPAIRE.B	* PPAIRE.H		
001	PPAIREO.B	PPAIREO.H		* PPAIREO.W
010	PPAIROE.B	PPAIROE.H		* PPAIROE.W
011	PPAIRO.B	PPAIRO.H		* PPAIRO.W
100				
101				
110				
111				



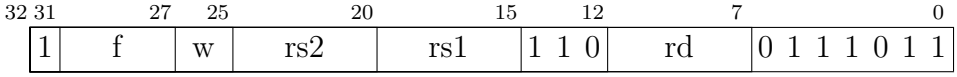
RV32	w			
f	00	01	10	11
000	{ PSRL.H }	*	{ PSRL.B }	
001				
010				
011				
100	{ PSRA.H }	*	{ PSRA.B }	
101				
110				
111				

RV64	w			
f	00	01	10	11
000	{ PSRL.H }	* { PSRL.W }	{ PSRL.B }	
001				
010				
011				
100	{ PSRA.H }	* { PSRA.W }	{ PSRA.B }	
101				
110				
111				



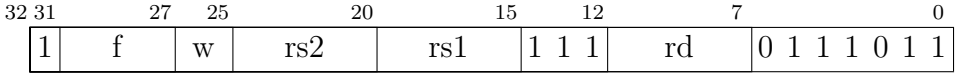
RV32	w			
f	00	01	10	11
0000	PM2ADD.H	*	PM4ADD.B	*
0001	PM2ADDA.H	*	PM4ADDA.B	*
0010	PM2ADD.HX	*		
0011	PM2ADDA.HX	*		
0100	PM2ADDU.H	*	PM4ADDU.B	*
0101	PM2ADDAU.H	*	PM4ADDAU.B	*
0110	PMQ2ADD.H	*	PMQR2ADD.H	*
0111	PMQ2ADDA.H	*	PMQR2ADDA.H	*
1000	PM2SUB.H	*	PM2SADD.H	
1001	PM2SUBA.H	*		
1010	PM2SUB.HX	*	PM2SADD.HX	
1011	PM2SUBA.HX	*		
1100	PM2ADDSU.H	*	PM4ADDSU.B	*
1101	PM2ADDASU.H	*	PM4ADDASU.B	*
1110				
1111	* MQACC.H01	*	* MQRACC.H01	*

RV64	w			
f	00	01	10	11
0000	PM2ADD.H	* PM2ADD.W	PM4ADD.B	* PM4ADD.H
0001	PM2ADDA.H	* PM2ADDA.W	PM4ADDA.B	* PM4ADDA.H
0010	PM2ADD.HX	* PM2ADD.WX		
0011	PM2ADDA.HX	* PM2ADDA.WX		
0100	PM2ADDU.H	* PM2ADDU.W	PM4ADDU.B	* PM4ADDU.H
0101	PM2ADDAU.H	* PM2ADDAU.W	PM4ADDAU.B	* PM4ADDAU.H
0110	PMQ2ADD.H	* PMQ2ADD.W	PMQR2ADD.H	* PMQR2ADD.W
0111	PMQ2ADDA.H	* PMQ2ADDA.W	PMQR2ADDA.H	* PMQR2ADDA.W
1000	PM2SUB.H	* PM2SUB.W	PM2SADD.H	
1001	PM2SUBA.H	* PM2SUBA.W		
1010	PM2SUB.HX	* PM2SUB.WX	PM2SADD.HX	
1011	PM2SUBA.HX	* PM2SUBA.WX		
1100	PM2ADDSU.H	* PM2ADDSU.W	PM4ADDSU.B	* PM4ADDSU.H
1101	PM2ADDASU.H	* PM2ADDASU.W	PM4ADDASU.B	* PM4ADDASU.H
1110				
1111	* PMQACC.W.H01	* MQACC.W01	* PMQRACC.W.H01	* MQRACC.W01



RV32	w			
f	00	01	10	11
0000	PAS.HX	*	PSA.HX	*
0001				
0010	PSAS.HX	*	PSSA.HX	*
0011	PAAS.HX	*	PASA.HX	*
0100				
0101				
0110				
0111				
1000	PMSEQ.H	* MSEQ	PMSEQ.B	
1001				
1010	PMSLT.H	* MSLT	PMSLT.B	
1011	PMSLTU.H	* MSLTU	PMSLTU.B	
1100	PMIN.H	*	PMIN.B	
1101	PMINU.H	*	PMINU.B	
1110	PMAX.H	*	PMAX.B	
1111	PMAXU.H	*	PMAXU.B	

RV64	w			
f	00	01	10	11
0000	PAS.HX	* PAS.WX	PSA.HX	* PSA.WX
0001				
0010	PSAS.HX	* PSAS.WX	PSSA.HX	* PSSA.WX
0011	PAAS.HX	* PAAS.WX	PASA.HX	* PASA.WX
0100				
0101				
0110				
0111				
1000	PMSEQ.H	* PMSEQ.W	PMSEQ.B	
1001				
1010	PMSLT.H	* PMSLT.W	PMSLT.B	
1011	PMSLTU.H	* PMSLTU.W	PMSLTU.B	
1100	PMIN.H	* PMIN.W	PMIN.B	
1101	PMINU.H	* PMINU.W	PMINU.B	
1110	PMAX.H	* PMAX.W	PMAX.B	
1111	PMAXU.H	* PMAXU.W	PMAXU.B	

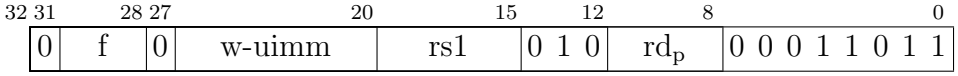


RV32	w			
f	00	01	10	11
0000	PMULH.H	*	PMULHR.H	* MULHR
0001	PMHACC.H	* MHACC	PMHRACC.H	* MHRACC
0010	PMULHU.H	*	PMULHRU.H	* MULHRU
0011	PMHACCU.H	* MHACCU	PMHRACCU.H	* MHRACCU
0100	PMULH.H.B0	* MULH.H0	PMULHSU.H.B0	* MULHSU.H0
0101	PMHACC.H.B0	* MHACC.H0	PMHACCSU.H.B0	* MHACCSU.H0
0110	PMULH.H.B1	* MULH.H1	PMULHSU.H.B1	* MULHSU.H1
0111	PMHACC.H.B1	* MHACC.H1	PMHACCSU.H.B1	* MHACCSU.H1
1000	PMULHSU.H	*	PMULHRSU.H	* MULHRSU
1001	PMHACCSU.H	* MHACCSU	PMHRACCSU.H	* MHRACCSU
1010	PMULQ.H	* MULQ	PMULQR.H	* MULQR
1011				
1100				
1101	* MQACC.H00	*	* MQRACC.H00	*
1110				
1111	* MQACC.H11	*	* MQRACC.H11	*

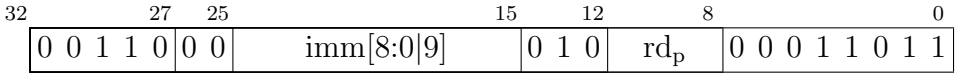
RV64	w			
f	00	01	10	11
0000	PMULH.H	* PMULH.W	PMULHR.H	* PMULHR.W
0001	PMHACC.H	* PMHACC.W	PMHRACC.H	* PMHRACC.W
0010	PMULHU.H	* PMULHU.W	PMULHRU.H	* PMULHRU.W
0011	PMHACCU.H	* PMHACCU.W	PMHRACCU.H	* PMHRACCU.W
0100	PMULH.H.B0	* PMULH.W.H0	PMULHSU.H.B0	* PMULHSU.W.H0
0101	PMHACC.H.B0	* PMHACC.W.H0	PMHACCSU.H.B0	* PMHACCSU.W.H0
0110	PMULH.H.B1	* PMULH.W.H1	PMULHSU.H.B1	* PMULHSU.W.H1
0111	PMHACC.H.B1	* PMHACC.W.H1	PMHACCSU.H.B1	* PMHACCSU.W.H1
1000	PMULHSU.H	* PMULHSU.W	PMULHRSU.H	* PMULHRSU.W
1001	PMHACCSU.H	* PMHACCSU.W	PMHRACCSU.H	* PMHRACCSU.W
1010	PMULQ.H	* PMULQ.W	PMULQR.H	* PMULQR.W
1011				
1100				
1101	* PMQACC.W.H00	* MQACC.W00	* PMQRACC.W.H00	* MQRACC.W00
1110				
1111	* PMQACC.W.H11	* MQACC.W11	* PMQRACC.W.H11	* MQRACC.W11

3 Encodings of instructions with one or more register-pair operands (RV32 only)

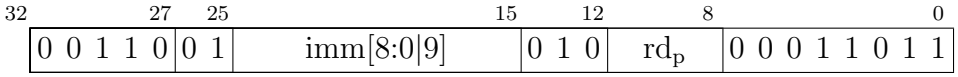
As before, where an instruction name is within braces { }, there is no such instruction proposed for the Base P extension, but the indicated encoding is recommended should the instruction be provided by another extension.



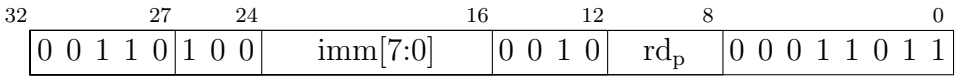
RV32 f	w-uimm 000xxxx	001xxxx	01xxxxx	1xxxxxx
000		PWSLLI.B	PWSLLI.H	WSLLI
001				
010				
011	*PLI instructions*			
100		PWSLAI.B	PWSLAI.H	WSLAI
101				
110				
111	*PLUI instructions*			



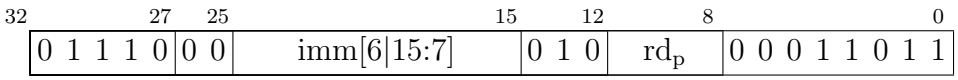
PLI.DH



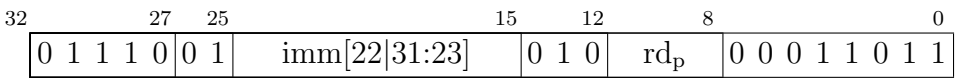
{ PLI.DW }



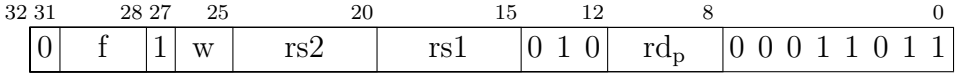
PLI.DB



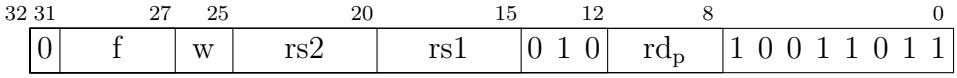
PLUI.DH



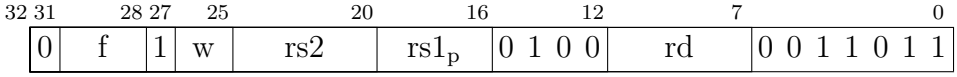
{ PLUI.DW }



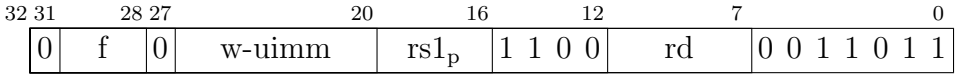
RV32 f	w 00	01	10	11
000	PWSLL.BS	PWSLL.HS		WSLL
001				
010				
011				
100	PWSLA.BS	PWSLA.HS		WSLA
101				
110				
111	WZIP8P	WZIP16P		



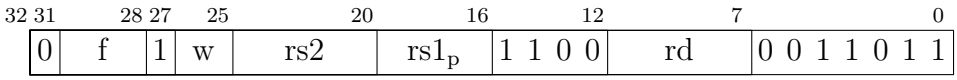
RV32 f	w 00	01	10	11
0000	PWADD.H	WADD	PWADD.B	PM2WADD.H
0001	PWADDA.H	WADDA	PWADDA.B	PM2WADDA.H
0010	PWADDU.H	WADDU	PWADDU.B	PM2WADD.HX
0011	PWADDAU.H	WADDAU	PWADDAU.B	PM2WADDA.HX
0100	PWMUL.H	WMUL	PWMUL.B	PM2WADDU.H
0101	PWMACC.H	WMACC	{ PWMACC.B }	PM2WADDAU.H
0110	PWMULU.H	WMULU	PWMULU.B	
0111	PWMACCU.H	WMACCU	{ PWMACCU.B }	
1000	PWSUB.H	WSUB	PWSUB.B	PM2WSUB.H
1001	PWSUBA.H	WSUBA	PWSUBA.B	PM2WSUBA.H
1010	PWSUBU.H	WSUBU	PWSUBU.B	PM2WSUB.HX
1011	PWSUBAU.H	WSUBAU	PWSUBAU.B	PM2WSUBA.HX
1100	PWMULSU.H	WMULSU	PWMULSU.B	PM2WADDSU.H
1101	PWMACCSU.H	WMACCSU	{ PWMACCSU.B }	PM2WADDASU.H
1110				
1111	PMQWACC.H	MQWACC	PMQRWACC.H	MQRWACC



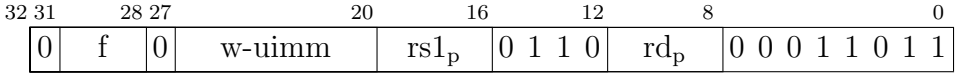
RV32 f	w 00	01	10	11
000				
001	PREDSUM.DHS		PREDSUM.DBS	
010				
011	PREDSUMU.DHS		PREDSUMU.DBS	
100				
101				
110				
111				



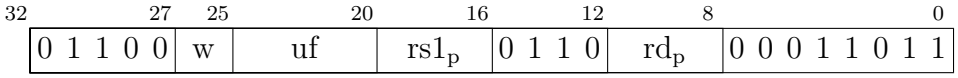
RV32 f	w-uimm 000xxxx	001xxxx	01xxxxx	1xxxxxx
000		PNSRLI.B	PNSRLI.H	NSRLI
001		{PNSRLRI.B}	{PNSRLRI.H}	{NSRLRI}
010		PNCLIPIU.B	PNCLIPIU.H	NCLIPIU
011		PNCLIPRIU.B	PNCLIPRIU.H	NCLIPRIU
100		PNSRAI.B	PNSRAI.H	NSRAI
101		PNSRARI.B	PNSRARI.H	NSRARI
110		PNCLIPI.B	PNCLIPI.H	NCLIPI
111		PNCLIPRI.B	PNCLIPRI.H	NCLIPRI



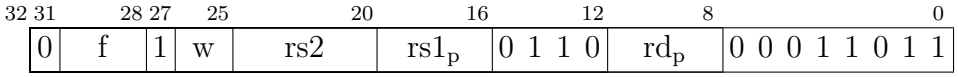
RV32 f	w 00	01	10	11
000	PNSRL.BS	PNSRL.HS		NSRL
001	{PNSRLR.BS}	{PNSRLR.HS}		{NSRLR}
010	PNCLIPU.BS	PNCLIPU.HS		NCLIPU
011	PNCLIPRU.BS	PNCLIPRU.HS		NCLIPRU
100	PNSRA.BS	PNSRA.HS		NSRA
101	PNSRAR.BS	PNSRAR.HS		NSRAR
110	PNCLIP.BS	PNCLIP.HS		NCLIP
111	PNCLIPR.BS	PNCLIPR.HS		NCLIPR



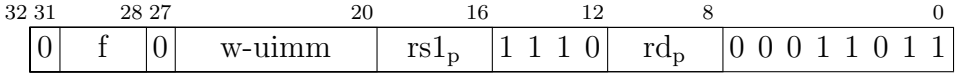
RV32 f	w-uimm 0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSLLI.DB	PSLLI.DH	PSLLI.DW	
001		{ PSSLLI.DB }	{ PSSLLI.DH }	{ PSSLLI.DW }	
010					
011					
100					
101		{ PSSLAI.DB }	PSSLAI.DH	PSSLAI.DW	
110	*unary instructions*				
111					



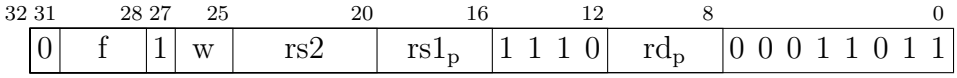
RV32 uf	w 00	01	10	11
00000	{ PCLZ.DH }	{ PCLZ.DW }	{ PCLZ.DB }	
00001				
00010				
00011	{ PCLS.DH }	{ PCLS.DW }	{ PCLS.DB }	
00100	PSEXT.DH.B	PSEXT.DW.B		
00101		PSEXT.DW.H		
00110				
00111	PSABS.DH	{ PSABS.DW }	PSABS.DB	
01000				
01001				
01010				
01011				
...				
11111				



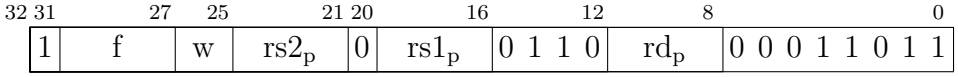
RV32 f	w 00	01	10	11
000	PSLL.DHS	PSLL.DWS	PSLL.DBS	
001	PADD.DHS	PADD.DWS	PADD.DBS	
010	PSSHL.DHS	PSSHL.DWS	{ PSSHL.DBS }	
011	PSSHLR.DHS	PSSHLR.DWS	{ PSSHLR.DBS }	
100				
101				
110	PSSHA.DHS	PSSHA.DWS	{ PSSHA.DBS }	
111	PSSHAR.DHS	PSSHAR.DWS	{ PSSHAR.DBS }	



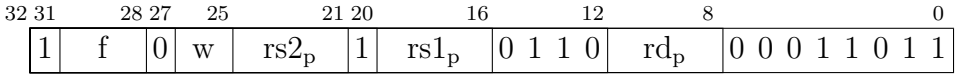
RV32 f	w-uimm				
	0000xxx	0001xxx	001xxxx	01xxxxx	1xxxxxx
000		PSRLI.DB	PSRLI.DH	PSRLI.DW	
001		{ PSRLRI.DB }	{ PSRLRI.DH }	{ PSRLRI.DW }	
010		{ PUSATI.DB }	PUSATI.DH	PUSATI.DW	
011					
100		PSRAI.DB	PSRAI.DH	PSRAI.DW	
101		{ PSRARI.DB }	PSRARI.DH	PSRARI.DW	
110		{ PSATI.DB }	PSATI.DH	PSATI.DW	
111					



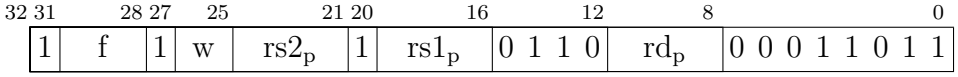
RV32 f	w			
	00	01	10	11
000	PSRL.DHS	PSRL.DWS	PSRL.DBS	
001				
010				
011				
100	PSRA.DHS	PSRA.DWS	PSRA.DBS	
101				
110				
111				



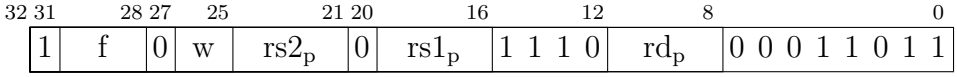
RV32	w			
f	00	01	10	11
0000	PADD.DH	PADD.DW	PADD.DB	ADDD
0001				
0010	PSADD.DH	PSADD.DW	PSADD.DB	
0011	PAADD.DH	PAADD.DW	PAADD.DB	
0100				
0101				
0110	PSADDU.DH	PSADDU.DW	PSADDU.DB	
0111	PAADDU.DH	PAADDU.DW	PAADDU.DB	
1000	PSUB.DH	PSUB.DW	PSUB.DB	SUBD
1001	PABD.DH	{ PABD.DW }	PABD.DB	
1010	PSSUB.DH	PSSUB.DW	PSSUB.DB	
1011	PASUB.DH	PASUB.DW	PASUB.DB	
1100				
1101	PABDU.DH	{ PABDU.DW }	PABDU.DB	
1110	PSSUBU.DH	PSSUBU.DW	PSSUBU.DB	
1111	PASUBU.DH	PASUBU.DW	PASUBU.DB	



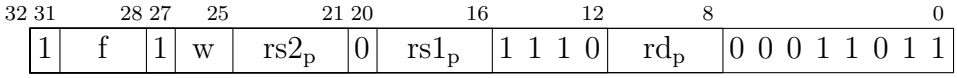
RV32	w			
f	00	01	10	11
000				
001				
010	PSH1ADD.DH	PSH1ADD.DW		
011	PSSH1SADD.DH	PSSH1SADD.DW		
100				
101				
110				
111				



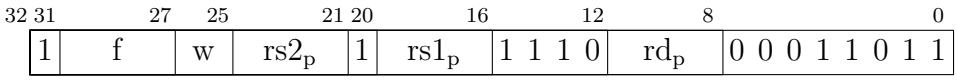
RV32	w			
f	00	01	10	11
000	{ PSLL.DH }	{ PSLL.DW }	{ PSLL.DB }	
001				
010	{ PSSHL.DH }	{ PSSHL.DW }	{ PSSHL.DB }	
011	{ PSSHLR.DH }	{ PSSHLR.DW }	{ PSSHLR.DB }	
100				
101				
110	{ PSSHA.DH }	{ PSSHA.DW }	{ PSSHA.DB }	
111	{ PSSHAR.DH }	{ PSSHAR.DW }	{ PSSHAR.DB }	



RV32	w			
f	00	01	10	11
000	PPAIRE.DB	PPAIRE.DH		
001	PPAIREO.DB	PPAIREO.DH		
010	PPAIROE.DB	PPAIROE.DH		
011	PPAIRO.DB	PPAIRO.DH		
100				
101				
110				
111				



RV32	w			
f	00	01	10	11
000	{PSRL.DH}	{PSRL.DW}	{PSRL.DB}	
001				
010				
011				
100	{PSRA.DH}	{PSRA.DW}	{PSRA.DB}	
101				
110				
111				



RV32	w			
f	00	01	10	11
0000	PAS.DHX		PSA.DHX	
0001				
0010	PSAS.DHX		PSSA.DHX	
0011	PAAS.DHX		PASA.DHX	
0100				
0101				
0110				
0111				
1000	PMSEQ.DH	PMSEQ.DW	PMSEQ.DB	
1001				
1010	PMSLT.DH	PMSLT.DW	PMSLT.DB	
1011	PMSLTU.DH	PMSLTU.DW	PMSLTU.DB	
1100	PMIN.DH	PMIN.DW	PMIN.DB	
1101	PMINU.DH	PMINU.DW	PMINU.DB	
1110	PMAX.DH	PMAX.DW	PMAX.DB	
1111	PMAXU.DH	PMAXU.DW	PMAXU.DB	